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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,736	01/23/2002	Satoshi Ikeda	SON-2313	3283

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RADER FISHMAN & GRAUER PLLC
LION BUILDING
1233 20TH STREET N.W., SUITE 501
WASHINGTON, DC 20036

EXAMINER	
KERVEROS, JAMES C	
ART UNIT	PAPER NUMBER
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/052,736	IKEDA, SATOSHI	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3 and 6-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3 and 6-32* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The reply brief filed on 08/17/2005 has been entered as a RESPONSE AFTER NON-FINAL ACTION under 37 CFR 1.111, since the Office Action mailed on 06/17/2005 is a Non-Final action due to a new ground of rejection initiated by the Examiner, and not an Examiner's Answer as deemed by the Applicant. Accordingly, an appeal conference is not mandatory in this case, if the examiner charged with the responsibility of preparing the examiner's answer reaches a conclusion that the appeal should not go forward and the supervisory patent examiner (SPE) approves, then no appeal conference is necessary. In this case, the examiner may reopen prosecution and issue another Office action. (See, MPEP § 1205, 1207.01 and 1207.04).

In view of the Reply Brief (Response under 37 CFR 1.111) filed on 8/17/2005, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth

in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

Claims 1, 3, 4 and 5 have been cancelled. Claims 3 and 6-32 are currently pending in this application, with claims 3, 6 and 22 being independent.

Prior Office Action Objection/Rejection

Objection to claims 3, 6-21 for reciting the term "adapted to" has been withdrawn, as indicated in the RESPONSE TO PETITION UNDER 37 C.F.R. 4 1.181 mailed 9/12/2005, responsive to Applicant's arguments in the PETITION UNDER 37 C.F.R. 4 1.181, filed 8/17/2005, REQUESTING WITHDRAWAL OF THE CLAIM OBJECTIONS in the Office Action mailed 6/17/2005.

The Examiner is hereby withdrawing the rejection of Claim 3 under 35 U.S.C. 112, second paragraph, with respect to claimed phrase "such a manner" for rendering the claim indefinite, in view of Applicant's arguments.

Response to Arguments

Applicant's arguments, in the reply brief filed 08/17/2005, with respect to the rejection of claims 3 and 6-32 under 35 U.S.C. 103(a) as being unpatentable over Satoh (U.S. Patent No. 6,477,672) in view of Kurosaki (U.S. Patent No. 6,314,536), have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

However, upon further consideration, a new ground of rejection of Claims 3 and 6-32 is made under 35 U.S.C. 102(e) as being anticipated by Reichert (US Patent No. 6,553,529), as set forth in the present Office Action, below.

In response to Applicant's argument, with respect to claim 3, the Examiner agrees with the Applicant's assertion that Kurosaki fails to disclose, teach, or suggest the pattern generator 2 producing the two burst address signals. However, under a new ground of rejection, Reichert discloses a pattern generator 24 having respective high-speed and low-speed modes for selectively producing test patterns according to the pattern memory for application to the device-under-test according to a DUT clock period. The high-speed, which corresponds to the narrow cycle period rate, is grater than a predetermined rate (>250 MHz), as set forth in the present Office Action.

Claims 3 and 6-32 are moot in view of a new ground of rejection.

Claim Objections

Claim 3 is objected to because of the following informalities:

Claim 3, the limitation in the last paragraph should be changed as follows:

"wherein said control means controls the timing of generation of the test pattern in such a manner that the cycle period ~~rate~~ to execute the test pattern of the desired address becomes a cycle period narrower than a predetermined ~~rate~~ cycle period" for consistency with the definition of a cycle period, since a cycle period rate refers to frequency being faster or slower or higher or lower, while a cycle period refers to the time duration of a cycle being shorter or longer or narrowing or widening.

Alternative, if Applicant chooses: "wherein said control means controls the timing of generation of the test pattern in such a manner that the cycle period rate to execute the test pattern of the desired address becomes a cycle period rate narrower than a predetermined rate". However, the first suggestion is more appropriate, because a cycle period is normally associated with narrowing or widening, as recited in passim in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 3 and 6-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Reichert (US Patent No. 6,553,529), filed: July 23, 1999.

Regarding independent Claims 3, 6, 22, Reichert discloses a semiconductor testing apparatus and method, Fig. 1, wherein an input signal of a test pattern from a pattern generation circuit 24 is supplied to a semiconductor device-under-test (DUT) 28

and an output signal obtained from the DUT 28 is compared with a prescribed expected in a failure processing circuit 50, comprising:

Test pattern memory means (a pattern memory) in a workstation 22, which operates as a test controller having a pattern memory and a user interface and a pattern generation circuit having respective high-speed and low-speed modes for selectively producing test patterns according to the pattern memory for application to the device-under-test according to a DUT clock period. A system bus connects to the test controller and the pattern generation circuit for routing command and data signals, Summary of the Invention and Fig. 1.

Test pattern generation means (pattern generator 24) for producing test patterns for application to the device-under-test 28. The pattern generator includes N pattern generators (only one shown in FIG. 1 for clarity) to generate a plurality of tester operating modes. The modes correspond to relatively high-speed (>250 MHz) and relatively slow-speed (<250 MHz) test patterns. A pin data line 27 and a global time set address line 29 are couple the pattern generator to the timing system while pattern information to and from the failure processor is distributed via the system bus 26.

Control means (test controller 22) for controlling the (pattern memory) and the (pattern generator 24) though the system bus 26, which connects to the test controller and the pattern generator for routing command and data signals. A timing system 30 includes producing the programmed timing signals necessary to fire per-pin drive/compare circuitry 42 at predetermined timings (defining a tester waveform) with respect to a period of operation for a device-under-test (DUT) 28.

Wherein the pattern generator 24 having respective high-speed and low-speed modes for selectively producing test patterns according to the pattern memory for application to the device-under-test according to a DUT clock period. The high-speed, which corresponds to the narrow cycle period rate, is grater than a predetermined rate (>250 MHz). Fig. 3 illustrates a high-speed test waveform suitable for application to a high-speed DUT pin as defined by timing signals generated by the timing system, and Fig. 5 further illustrates a portion of a multi-period waveform for application to a slow-speed DUT pin of around 200 MHz. The timing logic 34 includes a programmable PLL-based master oscillator MOSC 40 and a timing generator 45 that provides respective enable inputs to a plurality of edge generators in the form of respective interpolators EG0-EG12.

Regarding Claim 7, Reichert discloses decision means (failure processing circuit 50) to detect a failure within said semiconductor device DUT 28 by comparing an output test pattern signal received from the DUT with a first (test controller 22)

Regarding Claim 8, Reichert discloses control means (test controller 22) the programmable PLL-based master oscillator MOSC 40 that provides respective enable inputs to a plurality of edge generators in the form of respective interpolators EG0-EG12.

Regarding Claim 9, Reichert discloses first test pattern (test controller 22) is located at an address within the test pattern memory means (pattern memory) included in the workstation 22.

Regarding Claim 10, Reichert discloses semiconductor device DUT 28 is tested during the test pattern cycle period (DUT cycle), Figs. 3 and 5.

Regarding Claim 11-14, 23-25, Reichert discloses pattern generator 24 having respective high-speed and low-speed modes for selectively producing test patterns according to the pattern memory for application to the device-under-test according to a DUT clock period. The high-speed, which corresponds to the narrow cycle period rate, is grater than a predetermined rate (>250 MHz). Fig. 3 illustrates a high-speed test waveform suitable for application to a high-speed DUT pin as defined by timing signals generated by the timing system, and Fig. 5 further illustrates a portion of a multi-period waveform for application to a slow-speed DUT pin of around 200 MHz. The timing logic 34 includes a programmable PLL-based master oscillator MOSC 40 and a timing generator 45 that provides respective enable inputs to a plurality of edge generators in the form of respective interpolators EG0-EG12.

Regarding Claims 15-21, 26-32, Reichert discloses pattern generator including N pattern generators (only one shown in Fig. 1) to generate a plurality of tester operating modes, corresponding to relatively high-speed (>250 MHz) and relatively slow-speed (<250 MHz) test patterns. A pin data line 27 and a global time set address line 29 couple the pattern generator to the timing system while pattern information to and from the failure processor is distributed via the system bus 26. The timing system 30 includes timing logic 34 responsive to an edgiest memory 36 for producing the programmed timing signals necessary to fire per-pin drive/compare circuitry 42 at predetermined

timings (defining a tester waveform) with respect to a period of operation for a device-under-test (DUT) 28.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Primary Examiner
Art Unit 2138

Date: 24 January 2007
Office Action: Non-Final Rejection

U.S. Patent and Trademark Office
Alexandria, VA 22314
Tel: (571) 272-3824, Fax: (571) 273-3824
james.kerveros@uspto.gov

1/24/07

Albert Decady
Supervisory Patent Examiner

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100